Materials for Electronics

The U.S. electronics industry faces strong international competition in the manufacture of smaller, faster, more functional, and more reliable products. Many critical challenges facing the industry require the continual development of advanced materials and processes. The NIST Materials Science and Engineering Laboratory (MSEL) works closely with U.S. industry, covering a broad spectrum of sectors including semiconductor manufacturing, device components, packaging, data storage, and assembly, as well as complementary and emerging areas such as optoelectronics and organic electronics. MSEL has a multidivisional approach, committed to addressing the most critical materials measurement and standards issues for electronic materials. Our vision is to be the key resource within the Federal Government for materials metrology development and will be realized through the following objectives:

- Develop and deliver standard measurements and data for thin film and nanoscale structures;
- Develop advanced measurement methods needed by industry to address new problems that arise with the development of new materials;
- Develop and apply *in situ* as well as real-time, factory floor measurements for materials and devices having micrometer to nanometer scale dimensions;
- Develop combinatorial material methodologies for the rapid optimization of industrially important electronic and photonic materials;
- Provide fundamental understanding of the divergence of thin film and nanoscale material properties from their bulk values;
- Provide fundamental understanding, including first principles modeling, of materials needed for future nanoelectronic devices.

The NIST/MSEL program consists of projects led by the Metallurgy, Polymers, Materials Reliability, and Ceramics Divisions. These projects are conducted in collaboration with partners from industrial consortia (*e.g.*, SEMATECH), individual companies, academia, and other government agencies. The program is strongly coupled with other microelectronics programs within the government such as the National Semiconductor Metrology Program (NSMP). Materials metrology needs are also identified through the International Technology Roadmap for Semiconductors (ITRS), the International Packaging Consortium (IPC) Roadmap, the IPC Lead-free Solder Roadmap, the National Electronics Manufacturing Initiative (NEMI) Roadmap, the Optoelectronics Industry Development Association (OIDA) Roadmap, and the National Magnetic Data Storage Industry Consortium (NSIC) Roadmap.

MSEL researchers from each division have made substantial contributions to the most pressing technical challenges facing industry, from new fabrication methods and advanced materials in the semiconductor industry, to low-cost organic electronics, and to novel classes of electronic ceramics. Below are just a few examples of MSEL contributions over the past year.

Advanced Gate Dielectrics

To enable further device scaling, the capacitive equivalent thickness (CET) of the gate stack thickness must be 0.5 nm to 1.0 nm. This is not achievable with existing SiO_2/polcrystalline Si gate stacks. High dielectric constant gate insulators are needed to replace SiO_2, and metal gate electrodes are needed to replace polycrystalline Si. Given the large number of possible materials choices for the gate dielectric/substrate and gate dielectric/metal gate electrode interfaces, the MSEL Ceramics Division is establishing a dedicated combinatorial film deposition facility to study the complex interfacial interactions. This same methodology is applicable to a wide variety of problems in the electronic materials field.

Advanced Lithography

Lithography is the key enabling technology for the fabrication of advanced integrated circuits. As feature sizes decrease to sub-65 nm length scales, challenges arise because the image resolution and the thickness of the imaging layer approach the dimensions of the polymers used in the photoresist film. Unique high-spatial resolution measurements are developed to identify the limits of materials and processes for the development of photoresists for next-generation lithography.

Advanced Metallization

As the dimensions of copper metallization interconnects on microelectronic chips decrease below 100 nm, control of electrical resistivity becomes critical. The MSEL Metallurgy Division is developing seedless deposition methods that will simplify thin-film processing and result in film growth modes that increase trench filling, thus lowering interconnect resistivity.

Mechanical Reliability of Microchips

One of the important ITRS challenges is to achieve effective control of the failure mechanisms affecting chip reliability. Detection and characterization methods for dimensionally constrained materials will be critical to the attainment of this objective. Scientists in the MSEL Materials Reliability Division are addressing this issue by focusing on electrical methods capable of determining the thermal fatigue lifetime and mechanical strength of patterned metal film interconnects essential to microchips.

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